Workshop Manual

* Inverter

An inverter circuit outputs a voltage representing the opposite logic-level to its input. Its main function is to invert the input signal applied. If the applied input is low then the output becomes high and vice versa.

* Virtuoso in cadence

The Cadence® Virtuoso® System Design Platform is a holistic, system-based solution that provides the functionality to drive simulation and LVS-clean layout of ICs and packages from a single schematic. There are two key flows: implementation and analysis.

* Invertor Cell Layout

Cellular Layout? A cellular layout is the physical organization within a company that improves workflow, efficiency, and production. This structure entails the creation of work cells, which are micro units of 3-12 workers. Each unit contains a certain number of machines and supplies.

* Schematic Design

Schematic Design is the first phase of the architectural design process. The project team establishes the locations, physical specifications, and connections of all the necessary building spaces and components during the schematic design phase

* DRC

Design Rule Check (DRC) is the process of checking physical layout data against fabrication-specific rules specified by the foundry to ensure successful fabrication. Process specific design rules must be followed when drawing layouts to avoid any manufacturing defects during the fabrication of an IC.

* LVD Verification

The LVD test (Low Voltage Directive Test) is a test that confirms the compliance of CE marked devices with the CE marking criteria. The LVD test is a test that guarantees the safety of devices powered by electrical energy. LVD testing is done to prevent injuries from high voltage electrical shocks to devices.

* Parasitic Extraction

a parasitic extraction method is developed for the pre-route VLSI design. This method generates virtual route and estimates congestion using the placement information of standard cells, and then extract the interconnect parasitics with the pattern-library method.

* Post Layout Simulation

We have designed a layout from the schematic design (Layout/DRC). We have extracted that design (Extraction) and made sure both the schematic circuit and layout circuit match (LVS). Now, we have to simulate the extracted circuit. This is called Post Layout Simulation.

Workshop Manual

**This tutorial will guide you through various steps of LAYING out a CMOS inverter.**

**Introduction**

This document contains design guidelines for NT CMOS4S, a 1.2- micron, double polysilicon, double metal N-Well process.

**Various Layers in the CMOS Transistors**

CMOS transistors are made up of several layers. A brief summary of the MASKS used to generate these layers is given below. The reader can find an extended summary of these masks in the Layout Manual for CMOS4S, provided by CMC.

* N-Well
* Device Well
* P-Guard Exclusion
* Polysilicon
* Capacitor Polysilicon
* N+ Doping (Exclusion)
* P+ Doping (Inclusion)
* Contact Windows
* Metal 1
* Metal 2
* Via 1
* Passivation Windows

**Various Steps for Laying out an Inverter**

A CMOS inverter consists of both P-type and N-type MOS devices on the same common substrate. In the case of CMOS4s, we shall be dealing with an N-Well process. This implies that the substrate is of P-type and an N-Well must be etched into the P Substrate. When you open a window in df II, the plane of the screen represents the P-Substrate. The following steps show you how to layout both PMOS and NMOS on the P type substrate.

**LAYOUT OF A CMOS INVERTER**

* Place the device wells in the area which shall be active.

